

Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claims 1 to 11(Canceled):

12. (Currently Amended): A method of reducing an etch rate of a layer of liner oxide for a gate electrode, comprising the steps of:

providing a substrate, a gate electrode formed over said substrate, a liner oxide oxides with exposed surfaces formed over said substrate and on sidewalls of said gate electrode, and a gate spacer spacers formed on a portion of said liner oxide so that said liner oxide has an exposed surface not covered by said gate spacer; oxides;

nitridizing said exposed surface surfaces of said liner oxide oxides so as to form a layer of silicon oxy-nitride overlying said exposed surface of said liner oxide, said nitridizing step comprising an N₂/H₂ plasma exposure;

removing a portion of said liner oxide oxides not covered by said gate spacers and not covered by said layer of silicon oxy-nitride; and

saliciding contact points to said gate electrode.

13. (Currently Amended): The method of claim 12, said wherein said nitridizing step comprising a N₂/H₂ plasma exposure is applied applying nitridation to said a first and second surface surfaces of said layer of liner oxide comprising a N₂/H₂ and H₂ plasma exposure.

14. (Cancelled)

15. (Currently Amended): The method of claim 12, said wherein a layer of gate oxide is formed over said substrate, said gate oxide being created to a thickness between about 50 and 150 Angstrom.

16. (Currently Amended): The method of claim 12, said wherein said electrode layer of gate material comprising comprises polysilicon.

17. (Currently Amended): The method of claim 16-12, said wherein said electrodegate material being is deposited to a thickness between about 3,000 and 7,000 Angstrom.

18. (Canceled)

19. (Canceled)

20. (Currently Amended): The method of claim 12, said wherein said layer of liner oxide being created to has a thickness between about 100 and 500 Angstrom.

21. (Currently Amended): The method of claim 12, said wherein said salicidizing contact points to said with said gate electrode being is a cobalt base process of salicidation.

22. (Currently Amended): A method of reducing an etch rate of a layer of liner oxide for a gate electrode, comprising the steps of:

providing a substrate, a gate electrode formed over said substrate, a liner oxide oxides with exposed surfaces formed over said substrate and on sidewalls of said gate electrode, and a gate spacer spacers formed on said a portion of said liner oxide oxides so that said liner oxide has an exposed surface not covered by said gate spacer;

nitridizing said exposed surfacesurfaces of said liner oxideoxides so as to form a layer of silicon oxy-nitride overlying said exposed surface of said liner oxideoxides, said nitridizing step comprising an N₂/H₂ plasma exposure:

removing a portion of said liner oxideoxides not covered by said gate spacers and not covered by said layer of silicon oxy-nitride to leave a portion of said liner oxide beneath said gate spacers substantially without forming undercuts under said gate spacers; and
saliciding contact points to said gate electrode.

23. (Currently Amended): The method of claim 22, said wherein a layer of gate oxide being is formed over said substrate, said gate oxide having created to a thickness between about 50 and 150 Angstrom.

24. (Currently Amended): The method of claim 22, said wherein said gate electrode layer of gate material comprising comprises polysilicon.

25. (Currently Amended): The method of claim 24, said wherein said gate electrode material being is deposited to a thickness between about 3,000 and 7,000 Angstrom.

26. (Canceled)

27. (Canceled)

28. (Currently Amended): The method of claim 22, wherein said layer of liner oxide being created to has a thickness between about 100 and 500 Angstrom.

29. (Currently Amended): The method of claim 22, said wherein said saliciding contact points to said with said gate electrode being is a cobalt base process of salicidation.

30. (Currently Amended): The method of claim 22, wherein said nitridizing step comprising
a N₂/H₂ plasma exposure is applied to said a first and second surface surfaces of said layer of
liner oxide, comprising a N₂ and H₂ plasma exposure.

31. (Currently Amended): A method of reducing an etch rate of a layer of liner oxide for a gate electrode, comprising the steps of:

providing a substrate, a gate electrode formed over said substrate, a liner oxide~~oxides with exposed surfaces~~ formed over said substrate and on sidewalls of said gate electrode, and a gate spacers~~spacers~~ formed on said a portion of said liner oxide~~oxides~~ so that said liner oxide has an exposed surface not covered by said gate spacer;

nitridizing said exposed surfaces~~surfaces~~ of said liner oxide so as to form a layer of silicon oxy-nitride overlying an exposed surface of said gate electrode, said nitridizing step comprising
an N₂/H₂ plasma exposure;

removing a portion of said liner oxide~~oxides~~ not covered by said gate spacers and not
covered by said layer of silicon oxy-nitride substantially without forming divots in~~on~~ said liner oxide beneath said gate spacers; and

saliciding contact points to said gate electrode.

32. (Currently Amended): The method of claim 31, wherein said nitridizing step comprising
a N₂/H₂ plasma exposure is applied~~said applying nitridation~~ to said a first and second
surfaces~~surfaces~~ of said layer of liner oxide, comprising a N₂ and H₂ plasma exposure.

33. (Currently Amended): The method of claim 31, wherein said a layer of gate oxide is
formed over said substrate, said gate oxide being created to~~has~~ a thickness between about 50
and 150 Angstrom.

34. (Currently Amended): The method of claim 31, wherein said layer of gate electrode material comprising comprises polysilicon.
35. (Currently Amended): The method of claim 34, wherein said gate electrode material being is deposited to a thickness between about 3,000 and 7,000 Angstrom.
36. (Canceled)
37. (Canceled)
38. (Currently Amended): The method of claim 31, wherein said layer of liner oxide being created to has a thickness between about 100 and 500 Angstrom.
39. (Currently Amended): The method of claim 31, said wherein said salicidizing contact points to said with said gate electrode being is a cobalt base process of salicidation.
40. (Canceled)